

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Duncan et al. : Date: September 12, 2003

Serial Number: Concurrent : Group Art Unit: Unknown

Filed: Concurrent : Examiner: Unknown

Title: PERIPHERAL INTERFACE : IBM CORPORATION  
SYSTEM HAVING DEDICATED Intellectual Property Law  
COMMUNICATION CHANNELS : MD90/201-1  
8501 IBM Drive  
: Charlotte, NC 28262

---

**INFORMATION DISCLOSURE STATEMENT (IDS) UNDER 37 CFR 1.97**

**Commissioner For Patents  
Washington, D. C. 20231**

Dear Sir:

The attached Form PTO-1449, and any attached foreign patent office search report, provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This IDS is submitted under:

X  37 CFR 1.97(b) - No Fee.

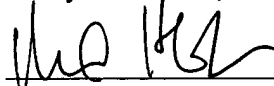
37 CFR 1.97(c) - No Fee. Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application. This communication is dated \_\_\_\_\_, which is not more than 3 months prior to the mailing of this statement.

37 CFR 1.97(c) - Fee.

37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge payments of any associated fees required under 37 CFR 1.17(p) and (i) (1) to Deposit Account No.09-0469 (IBM).

Respectfully submitted,

By:   
Michael F. Hoffman  
Registration No.: 40,019  
Telephone No.: (518) 449-0044

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.

CHA920030019US1

SERIAL NO.

Applicants: Duncan et al.

FILING

GROUP

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	US 2002/0191599 A1	12/2002	Parthasarathy et al.			
	US 2002/0170951 A1	11/2002	Oshins et al.			
	US 6,487,628 B1	11/2002	Duong et al.			
	US 6,175,889 B1	1/2001	Olarig			
	6,134,622	10/2000	Kapur et al.			
	5,991,824	11/1999	Strand et al.			

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	WO 02/35367 A1	5/2002	PCT				
	JP2003018188A	1/2003	JP				
	JP2000010912A	1/2000	JP				

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		"INFINIBAND: An End-User Perspective," Prepared by The Kent Row Group, date and source unknown, pp. 1-18.
		Leddy, W., "InfiniBand Software: Design Matters," Lane 15 Software, Inc., v 1.0, June 2001, pp. 1-9.

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

CHA920030019US1

Application Number

Applicant(s)

Duncan et al.

Filing Date

Group Art Unit

\*EXAMINER  
INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Paavola, S., "Embedded InfiniBand," A SKY Computers White Paper, www.skycomputers.com, date unknown.

Paavola, S., "InfiniBand Architecture Delivers Enhanced Reliability," A SKY Computers White Paper, www.skycomputers.com, date unknown.

Tanabe et al., "A Low Latency High Bandwidth Network Interface Prototype for PC Cluster," Int'l Workshop on Innovative Architecture for Future Generation High-Performance Processors and Systems, 10-11 Jan. 2002.

Tanabe et al., "A prototype of high bandwidth low latency network interface plugged into a DIMM slot," date and source unknown.

Duncan et al., "High Performance I/O Design in the AlphaServer 4100 Symmetric Multiprocessing System," Digital Tech. Journal, Vol. 8 No. 4, updated 25 April 1997, pp. 1-20.

Bouvier, D., "RapidIO: The Interconnect Architecture for High Performance Embedded Systems," www.rapidio.org, Jan. 2003, pp. 1-20.

Leroux, P., "Making the Switch to RapidIO: Using a Message-passing Microkernel OS to Realize the Full Potential of the RapidIO Interconnect," QNX Software Systems Ltd., 2002, pp. 1-11.

"The Lightning Data Transport I/O Bus Architecture," LDT Architecture White Paper Rev. 1001, Api NetWorks, Inc., 2000, pp. 1-18.

Lindenstruth, V., "Novel Intelligent I/O Architecture Eliminating the Bus Bottleneck," date and source unknown.

"Realizing the Full Potential of Server, Switch & I/O Blades with InfiniBand Architecture," White Paper, Mellanox Technologies, Inc., Dec. 2001, pp. 1-11.

Stigliani, Jr., et al., "IBM eServer z900 I/O Subsystem," IBM Journal of Research and Development, Vol. 46 No. 4/5, July/Sept. 2002, pp. 421-445.

"Technology Background," Intelligent-IO.com, author and date unknown.

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

CHA920030019US1

Application Number

Applicant(s)

Duncan et al.

Filing Date

Group Art Unit

\*EXAMINER  
INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Rosdahl, J., "The I2O Host Environment," Novell, Inc., date and source unknown.

Easley, M., "Processor Independent I2O Solutions Using Shell and Private Platform," www.plxtech.com.

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.